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	Subsystem/Office Calorimeter Subsystem	
Document Title **Calorimeter – LAT Interface Control Document**		

Gamma-ray Large Area Space Telescope (GLAST)

Large Area Telescope (LAT)

Interface Control Document between the Calorimeter Subsystem and LAT Instrument

CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes
D1	6/28/2001	First draft
D2	7/15/2002	Combined Electrical and Mech/Therm ICD's
D3	9/30/2002	Extensive rewrite
04	3/11/2003	Initial release

Table of Contents

1 PURPOSE

This document describes the interfaces of the CAL subsystem with the LAT instrument. It is intended to be used to document the interfaces, so subsystem components can be designed and fabricated, based on clear, understood values for their interfaces to the rest of the LAT. This ICD will also serve as the requirements list against which interface tests are developed, and against which the CAL subsystem must be verified prior to integration on the LAT.

2 SCOPE

This ICD includes all interfaces of the CAL subsystem to other components of the LAT instrument, including mechanical, electrical, and thermal.

3 ACRONYMS

ADC	Analog to Digital Converter
AFEE	Analog Front-End Electronics (Circuit Board)
ASIC	Application-Specific Integrated Circuit
CAL	LAT calorimeter subsystem
COTS	Commercial Off-the-Shelf
DAC	Digital to Analog Converter
EMI	Electromagnetic Interference
FOV	Field of View
FWHM	Full Width Half Maximum
GCFE	GLAST Calorimeter Front-End Electronics (ASIC)
GCRC	GLAST Calorimeter Readout Controller
GLAST	Gamma-ray Large Area Space Telescope
IRD	Interface Requirements Document
LAT	Large Area Telescope
PEM	Pre-Electronics Module
PSA	Power Supply Assembly
SI/SC IRD	Science Instrument – Spacecraft Interface Requirements Document
SRD	Science Requirements Document
TBR	To Be Resolved
TEM	Tower Electronics Module
TRG	L1 Trigger

4 DEFINITIONS

γ	Gamma Ray
μsec, μs	Microsecond, 10^{-6} second
A_{eff}	Effective Area
Analysis	A quantitative evaluation of a complete system and /or subsystems by review/analysis of collected data.
Arcmin	An arcmin is a measure of arc length. One arcmin is 1/60 degree.
Beam Test	Test conducted with high energy particle beams
cm	centimeter
Cosmic Ray	Ionized atomic particles originating from space and ranging from a single proton up to an iron nucleus and beyond.
Dead Time	Time during which the instrument does not sense or record gamma ray events during normal operations.
Demonstration	To prove or show, usually without measurement of instrumentation, that the project/product complies with requirements by observation of results.
eV	Electron Volt
Field of View	Integral of effective area over solid angle divided by peak effective area.
GeV	Giga Electron Volts. 10^{9} eV
Inspection	To examine visually or use simple physical measurement techniques to verify conformance to specified requirements.
MeV	Million Electron Volts, 10^{6} eV
μsec, μs	Microsecond, 10^{-6} second
ph	photons
s, sec	seconds
Simulation	To examine through model analysis or modeling techniques to verify conformance to specified requirements
sr	steradian, A steradian is the solid (3D) angle formed when an area on the surface of a sphere is equal to the square of the radius of the sphere. There are 4 Pi steradians in a sphere.
Testing	A measurement to prove or show, usually with precision measurements or instrumentation, that the project/product complies with requirements.
Validation	Process used to assure the requirement set is complete and consistent, and that each requirement is achievable.
Verification	Process used to ensure that the selected solutions meet specified requirements and properly integrate with interfacing products.

5 APPLICABLE DOCUMENTS

Documents that are relevant to the definition and functionality of CAL – LAT interfaces include the following:

ANSI Y 14.5M

GSFC-433-RQMT, "GLAST EMI/EMC Requirements Document"

LAT-MD-00404, "LAT Contamination Control Plan"

LAT-DS-00233, "CAL-LAT Interface Definition Drawing"

LAT-DS-01625, "Calorimeter Outline Drawing"

LAT-SS-00009, "GLAST LAT Science Requirements Document"

LAT-SS-00010, "GLAST LAT Performance Specification"

LAT-SS-00018, "LAT CAL Subsystem Specification – Level III Specification"

LAT-SS-00019, "LAT T&DF Subsystem Specification – Level III Specification"

LAT-SS-00088, "Calorimeter Front End (GCFE) ASIC Conceptual Design"

LAT-SS-00115, "LAT Mechanical Subsystem Specification – Level III Specification"

LAT-SS-00210, "LAT CAL Subsystem Specification – Level IV Specification"

LAT-SS-00208, "Calorimeter Readout Control (GCRC) ASIC Conceptual Design"

LAT-SS-00272, "Calorimeter Module Grounding and Shielding Plan"

LAT-SS-00278, "Calorimeter Analog Front End Electronics (AFEE) Board Specification"

LAT-SS-00291, "LAT Grounding and Shielding Plan"

LAT-SS-00778, "LAT Environmental Specification"

LAT-TD-00035, "LAT Coordinate and Numbering Systems"

LAT-TD-00242, "Calorimeter Subsystem Preliminary Design Report"

6 MECHANICAL INTERFACES

6.1 General Description

The CAL-Grid interface is the primary mechanical interface for the CAL. This provides the structural support for the CAL, and provides a stable reference by which the CAL position is surveyed and maintained. This interface also provides the primary means by which heat generated in the CAL module is conducted out to the Radiators.

The CAL base plate is designed to provide additional stiffness to the LAT Grid and is also the primary mechanical interface for the Tower Electronics Module (TEM) and TEM Power Supply (TPS). Four stand-offs, as described in the CAL-LAT IDD, LAT-DS-00233, are between the CAL base plate and the TEM to achieve the required thermal isolation. The electrical interface for each CAL module is to the TEM and TPS subsytems mounted on each CAL module base plate.

Integration interfaces are also on the CAL base plate. These include four tapped holes used for GSE to support and integrate the module in the Grid.

The reference coordinate system is shown in LAT Coordinate System, LAT-TD-00035.

The System of Units used shall be metric.

Any drawings included in this document or refered to shall meet ANSI Y14.5M standards.

6.2 Flight Hardware

6.2.1 Calorimeter Responsibilities

Development, fabrication, and test of the Calorimeter subsystem with mechanical, electrical and thermal characteristics identified in this ICD. In particular, the CAL bottom plate with sufficient stiffness and strength and with tab details and features as described in the CAL-LAT Interface Definition Drawing (IDD), LAT-DS-00233.

6.2.2 LAT Responsibilities

- Development, fabrication, and test of the LAT grid, mounting bolts, washers, and Grid threaded inserts for CAL module mounting to the grid. (Mechanical Systems responsibility)
- Procurement and installation of CAL mounting bolts, washers, Grid inserts, and any thermal contact tape at the interface. (Mechanical Systems responsibility).
- Design and test of TEM – CAL standoffs. (Mechanical Systems responsibilty).
- Fabrication and/or procurement of the TEM – CAL standoffs, mounting bolts, washers, and associated hardware for mounting of the TEMs to the CAL modules. (Electronics responsibility).
- Development, fabrication, and test of any brackets, clamps, and supports for electrical harnessing that crosses the CAL – LAT interface. (Electronics responsibility).
- Development, fabrication, and test of the TEMs and PSAs (Electronics responsibility).

6.3 Mass Properties

6.3.1 Mass (Reference Only)

The calorimeter subsystem mass allocation is 1440.0 kg (Mar 2003).

6.3.2 CAL Module Mass Variation

The maximum allowable mass variation among CAL modules shall be +/- 2 kg.

6.3.3 CAL Module Center of Gravity

The maximum X/Y center of gravity offset from the geometric center of a Cal module is +/- 10 mm.

The maximum Z center of gravity position from the CAL-grid interface is 116 mm.

6.4 Structural Mounting and Load Transfer

6.4.1 CAL Requirements

The Calorimeter mount to the Grid shall conform to the dimensions and tolerances shown in LAT-DS-00233. This describes the nominal dimensions and tolerances of the mounting tabs and holes on the CAL base plate.

The CAL base plate shall have the effective in-plane extensional stiffness of an aluminum plate 8 mm thick in the mounting plane with the Grid

The CAL base plate shall have the effective in-plane shear stiffness equivalent to an aluminum plate 8 mm thick, in the mounting plane with the Grid.

The CAL base plate shall have a CTE of 21-25 x 10^{-6} m/m/degC (consistent with rolled aluminum alloy plate).

The surface condition (coating, roughness, and planarity) of the CAL mounting tabs shall be as described in LAT-DS-00233, to effect the maximum possible friction at the bolted interface joint.

6.4.2 LAT Requirements

The Grid mounting surface for the CAL shall conform to the dimensions and tolerances shown in LAT-DS-00233 . This describes the nominal dimensions and tolerances of the mounting surface on the Grid, holes and threaded holes.

The grid structure shall have a CTE of 21-25 x 10^{-6} m/m/degC (consistent with rolled aluminum alloy material).

Four titanium stand-offs are between the CAL base plate and the TEM and shall conform to the dimensions and tolerances as shown in the CAL-LAT IDD, LAT-DS-00233,

6.5 Structural Limit Loads and Environmental Requirements

The LAT Environmental Specification, LAT-SS-00778, is the guiding document for defining environmental specifications. If there is a conflict of information between this ICD and the LAT Environmental Specification, the LAT Environmetal Specification will take precedence.

6.5.1 CAL Requirements

6.5.1.1 First Mode Frequency

The fixed base stiffness, fixed at the CAL Baseplate - Grid interface points, shall produce a first mode frequency greater than 50 Hz. (433-IRD-0001, 3.2.2.8.1.2)

6.5.1.2 Static-Equivalent Accelerations

Refer to LAT Environmental Specification, LAT-MD-00778-01, Section 8.1, Static-Equivalent Accelerations.

6.5.1.3 CAL—Grid Interface Loads on CAL Tabs

Refer to LAT Environmental Specification, LAT-MD-00778-01, Section 8.2, Interface Limit Loads.

6.5.1.4 CAL-Grid Interface Distorsion for Worst-Case Grid Bay

Refer to LAT Environmental Specification, LAT-MD-00778-01, Section 8.2, Interface Limit Loads.

6.5.1.5 Electronics Box-CAL Interface Loads

Refer to LAT Environmental Specification, LAT-MD-00778-01, Section 8.2, Interface Limit Loads.

6.5.1.6 Sinusoidal Vibration

Refer to LAT Environmental Specification, LAT-MD-00778-01, Section 9.1, Sinusoidal Vibration.

6.5.1.7 Random Vibration

Refer to LAT Environmental Specification, LAT-MD-00778-01, Section 9.2, Random Vibration.

6.5.1.8 Acoustic Spectrum

Refer to LAT Environmental Specification, LAT-MD-00778-01, Section 9.3, Acoustic.

6.5.1.9 Shock Environment

Refer to LAT Environmental Specification, LAT-MD-00778-01, Section 10, Shock Environment.

6.5.2 LAT Requirements

The Grid shall be capable of tolerating the reaction forces due to CAL acceleration loading.

The Grid shall be capable of tolerating the reaction forces due to CAL vibration loading.

During worst-case deflection of the Grid during launch, the CAL bolting surface shall distort no more than 0.1 mm.

Tapped holes for mounting the CAL shall tolerate a maximum load plus pre-load of 5000 N, without adverse affects on the threads or bolts.

7 DIMENSIONS

Stay-clear dimensions are not-to-exceed dimensions. The nominal dimensions plus any needed tolerances shall be included within this stay-clear. These dimensions are defined, and will be measured with respect to a unique datum reference system for each module. The datum reference is defined in LAT-DS-00233 CAL-LAT IDD.

7.1 Static Stay-Clear Dimensions

All stay-clears and dimensions shall be defined, toleranced, and measured with respect to the datum reference system defined in LAT-DS-00233, CAL-LAT IDD, unless explicitly defined otherwise.

CAL components shall stay within the stay-clear volume described in LAT-DS-00233. This volume includes the region for nominal dimensions and tolerances with respect to the datums described above.
Stay-clear dimensions shall be measured at 21 +/- 3 °C.

7.2 Dynamic Stay-Clear for Dynamic Motions

During launch and on-orbit operation, dynamic motions due to external loading may cause parts of a CAL module to violate the static stay-clear dimensions. Maximum excursions beyond the static stay-clears delineated above are:

Lateral (CAL): 0.5 mm in any direction (X or Y) (at top of module)

Vertical (CAL): 0.25 mm in either direction (+Z or –Z) (at center of module)

8 ELECTRICAL INTERFACES

8.1 Overview

The Calorimeter electronics consists of four Analog Front End Electronics (AFEE) cards that are mounted on the sides of the Pre-Electronics Module (PEM) between the inner closeout plates and outer side panels. Attached to each AFEE board is an interface cable assembly that combines the signals from two AFEE board connectors to a single TEM connector, which connects to the Tower Electronics Module (TEM) and Power Supply Assembly (PSA) mounted on the outside of the CAL Module as depicted in Figure 1. This interface cable assembly provides both signal and power connections between the AFEE and the TEM.

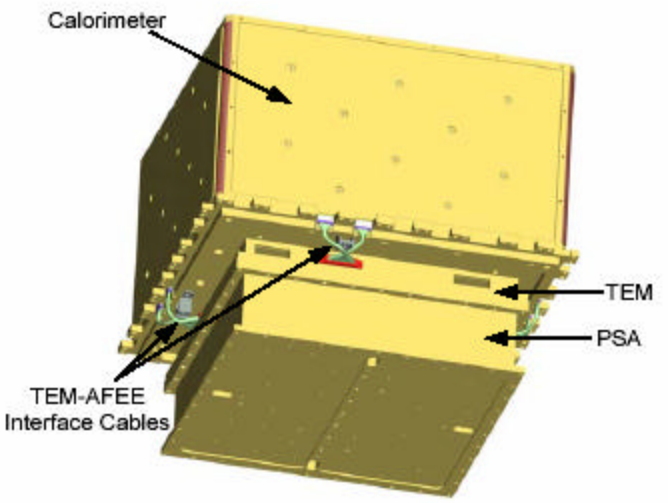


Figure 1: Calorimeter with TEM and PSA Attached

As shown in Figure 2, the four AFEE boards communicate with the Tower Electronics Module (TEM) that is mounted, along with the CAL power supply, underneath the PEM baseplate. The CAL controller, which is part of the TEM, merges the data from the four AFEE cards into a CAL event packet which is combined with Tracker and Trigger system data for transmission to the Trigger and Data Flow system for analysis.

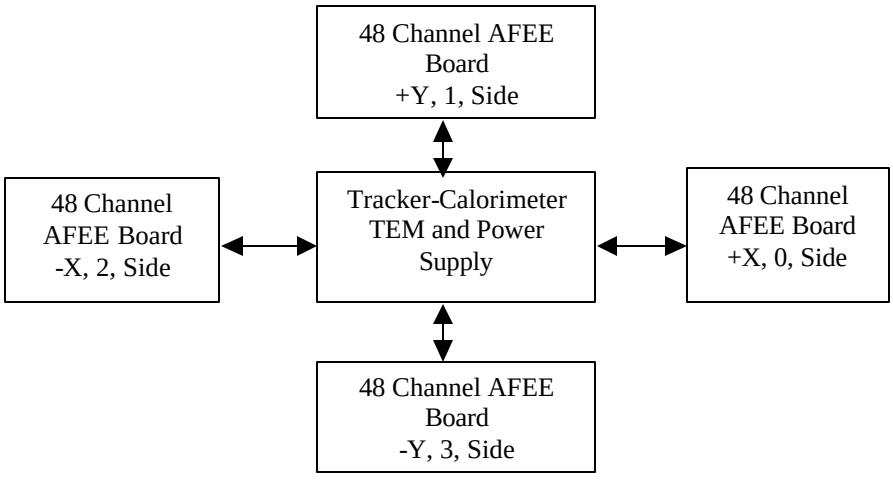


Figure 2: AFEE to TEM Layout

8.2 CAL Module – TEM Interface

The CAL Module interfaces to the TEM via four identical interface cables. Each cable is comprised of two connectors for mating with an AFEE card and one connector to mate to the TEM electronics. The interface cable is oriented as a "Y", combining signals from the two AFFE board connectors to a single connector for connection to the TEM.

8.2.1 TEM Module Connector

The connector on the TEM which mates to the CAL Module cable connector is a 69 pin micro-D receptacle, M83513 type, manufactured by Cristek Interconnects, Inc. or Airborn, Inc. The Cristek part number is MCR-1069-1B1. Figure 3 details the location of TEM Module connectors with relation to those on the CAL Module AFEE cards.

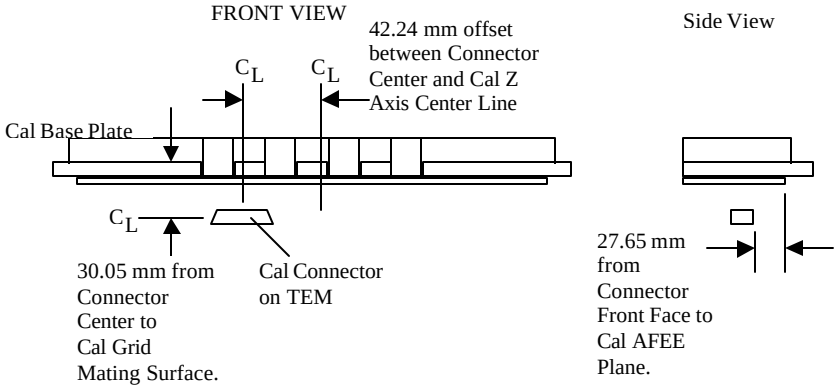
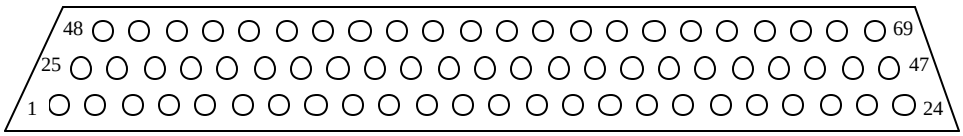


Figure 3: CAL Module Connector Interface

8.2.2 TEM Module Interface Cable Connector

The TEM interface cable connector is a 69-pin plug contact micro-D, M83513 type, manufactured by Airborn, Inc. The connector has low-profile hex jackscrews. The Airborn part number is MM-312-069-113-4100. The pin arrangement is illustrated in Figure 4.



69 Contact Receptacle Mating Face

Figure 4: TEM Connector Contact Arrangement

8.3 Signal Interfaces

Note that in signal naming, signals between the TEM and GCRC begin with the letters "CAL_" indicating Calorimeter subsystem. Additionally, signals that are asserted low, have an "N" prefix in the root name. For example, the signal name "CAL_NCMD" indicates it is a Command line (CMD) between the Calorimeter and TEM, asserted low. Output signals for which there is one per AFEE row have a suffix number indicating row. Lastly, differential signals have a suffix of either "P" denoting positive zero level or suffix "M" denoting minus zero level. For example, signal CAL_NTREQLE1P is a Calorimeter subsystem signal asserted low, from Layer 1 and is differential positive.

Also, note that unused pins that are grounded within the TEM will not be connected at the CAL Module.

8.3.1 Pin Assignments and Signal Descriptions

Table 1 provides CAL Module interface connector pin assignments and signal descriptions.

Table 1: TEM AFEE Assembly, Interface Connection Pin Assignment

Pin	Signal Name	Signal Description	AFEE In/Out
1	TEM Ground	Grounded at TEM, not connected in CAL module	N/A
2	CAL_NRESETP	Reset command from TEM -Bussed to all 4 GCRCs	Input
3	CAL_NRESETM		Input
4	CAL_NCMDP	Command from TEM - Bussed to all 4 GCRCs	Input
5	CAL_NCMDM		Input
6	CAL_CLKP	System Clock from TEM (20 MHz) - Bussed to all 4 GCRCs	Input
7	CAL_CLKM		Input
8	CAL_NTREQLE0P	L1 Low Energy Trigger Request, Cal Row 0, to TEM	Output
9	CAL_NTREQLE0M		Output
10	CAL_NTREQHE0P	L1 High Energy Trigger Request, Cal Row 0, Request to TEM	Output
11	CAL_NTREQHE0M		Output
12	CAL_NDATA0_0P	Data to TEM, “Pipe” 0 of Cal Row 0	Output
13	CAL_NDATA0_0M		Output
14	CAL_NDATA1_0P	Data to TEM, “Pipe” 1 of Cal Row 0	Output
15	CAL_NDATA1_0M		Output
16	CAL_NTREQLE1P	L1 Low Energy Trigger Request, Cal Row 1, to TEM	Output
17	CAL_NTREQLE1M		Output
18	CAL_NTREQHE1P	L1 High Energy Trigger Request, Cal Row 0, Request to TEM	Output
19	CAL_NTREQHE1M		Output
20	CAL_NDATA0_1P	Data to TEM, “Pipe” 0 of Cal Row 1	Output
21	CAL_NDATA0_1M		Output
22	Spare	Spare connection, unconnected	N/A
23	3.3V DIGITAL	Digital Supply, nominally 3.3 Volts	Power
24	3.3V DIGITAL	Digital Supply, nominally 3.3 Volts	Power
25	TEM Ground	Grounded at TEM, not connected in CAL module	N/A
26	TEM Ground	Grounded at TEM, not connected in CAL module	N/A
27	3.3V ANA RET	Analog Supply return	Power
28	CAL_NDATA1_1P	Data to TEM, “Pipe” 1 of Cal Row 1	Output
29	CAL_NDATA1_1M		Output
30	CAL_NTREQLE2P	L1 Low Energy Trigger Request, Cal Row 2, to TEM	Output
31	CAL_NTREQLE2M		Output
32	CAL_NTREQHE2P	L1 High Energy Trigger Request, Cal Row 0, Request to TEM	Output
33	CAL_NTREQHE2M		Output
34	CAL_NDATA0_2P	Data to TEM, “Pipe” 0 of Cal Row 2	Output
35	CAL_NDATA0_2M		Output
36	CAL_NDATA1_2P	Data to TEM, “Pipe” 1 of Cal Row 2	Output
37	CAL_NDATA1_2M		Output
38	CAL_NTREQLE3P	L1 Low Energy Trigger Request, Cal Row 3, to TEM	Output

Pin	Signal Name	Signal Description	AFEE In/Out
39	CAL_NTREQLE3M		Output
40	CAL_NTREQHE3P	L1 High Energy Trigger Request, Cal Row 0, Request to TEM	Output
41	CAL_NTREQHE3M		Output
42	CAL_NDATA0_3P	Data to TEM, "Pipe" 0 of Cal Row 3	Output
43	CAL_NDATA0_3M		Output
44	CAL_NDATA1_3P	Data to TEM, "Pipe" 1 of Cal Row 3	Output
45	CAL_NDATA1_3M		Output
46	DIG RET	Digital Supply return	Power
47	DIG RET	Digital Supply return	Power
48	TEM Ground	Grounded at TEM, not connected in CAL module	N/A
49	3.3V ANALOG	Analog Supply, nominally 3.3 Volts	Power
50	CAL_RIGHT_FIRST	Control Bit, Swaps log-end left/right readout order when asserted high Asserted by TEM	Input
51	CAL_RIGHT_RET	Return for Right First control	Power
52	3.3V ANALOG	Analog Supply, nominally 3.3 Volts	Power
53	3.3V ANALOG	Analog Supply, nominally 3.3 Volts	Power
54	ANA RET	Analog Supply return	Power
55	ANA RET	Analog Supply return	Power
56	CAL_THERM0P	Analog connection to Thermistor 0 for sensing AFEE board temperature	Output
57	CAL_THERM0M		Output
58	3.3V DIGITAL	Digital Supply, nominally 3.3 Volts	Power
59	3.3V DIGITAL	Digital Supply, nominally 3.3 Volts	Power
60	DIG RET	Digital Supply return	Power
61	DIG RET	Digital Supply return	Power
62	CAL_THERM1P	Analog connection to Thermistor 1 for sensing AFEE board temperature	Output
63	CAL_THERM1M		Output
64	BIAS RET	Bias Voltage Supply return	Power
65	BIAS RET	Bias Voltage Supply return	Power
66	BIAS VOLTAGE	High Voltage (70-100 Volts) Supply for PIN Photodiode bias	Power
67	BIAS VOLTAGE	High Voltage (70-100 Volts) Supply for PIN Photodiode bias	Power
68	BIAS VOLTAGE	High Voltage (70-100 Volts) Supply for PIN Photodiode bias	Power
69	BIAS RET	Bias Voltage Supply return	Power

8.3.1.1 RIGHT_FIRST Signal

The RIGHT_FIRST signal is used to control the left – right association on an AFEE board, so that two opposing AFEE board's (i.e. X+ and X-) log-ends are logically addressed the same. The RIGHT_FIRST addressing is used both in Register Read/Writes and range readout. Figure 5 shows that with opposing AFEEs having opposite RIGHT_FIRST assertions, an addressed command will be directed to the same log electronics. In a similar manner, for range readout, the data bits from both ends of the same crystal log will arrive at the TEM at the same time. Table 2 defines the level of the RIGHT_FIRST signal for each side of the CAL Module. A special filter circuit is used to minimize noise coupling between the TEM and AFEE cards, as shown in Figure 6, the RIGHT_FIRST signal interface description.

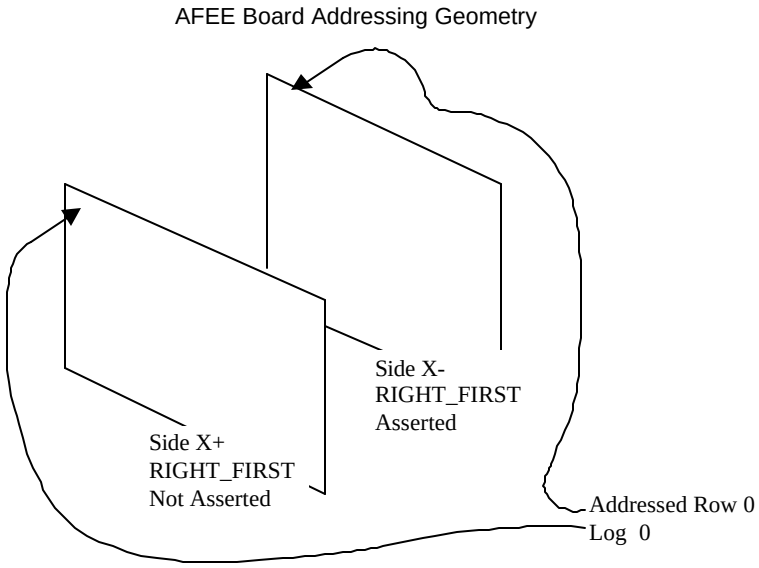


Figure 5: AFEE RIGHT_FIRST Signal Usage

AFEE Side	Assertion Level of RIGHT_FIRST
+X	Low
+Y	High, switch left - right addressing.
-X	High, switch left - right addressing.
-Y	Low

Table 2: RIGHT_FIRST Association Per AFEE Side

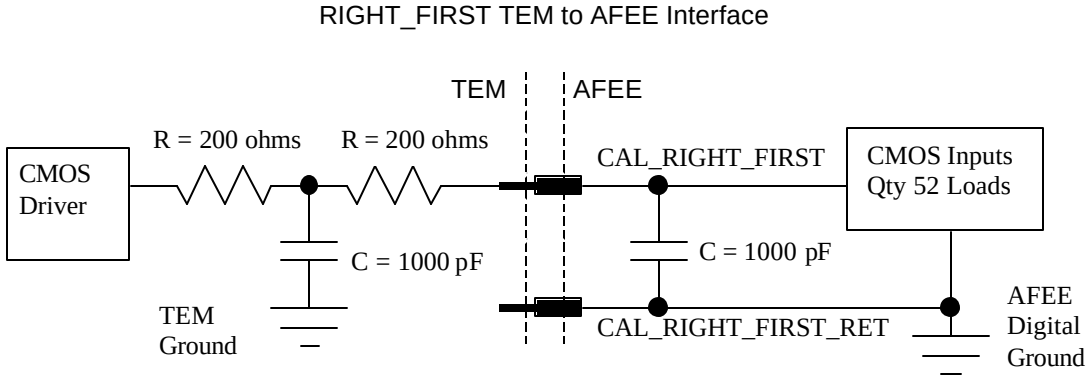


Figure 6: RIGHT_FIRST Signal Description

8.3.1.2 Trigger Request Signals

Trigger requests from the CAL Module to the TEM are on the CAL_NTREQHE and CAL_NTREQLE lines. The signaling format is minimum pulse width of 200 nsec, and maximum pulse length is time-over-threshold. The trigger communication lines between the GCRC and TEM are LVDS, asserted low.

8.4 Reset

Resets of the AFEE are performed on the CAL_NRESET input line or by TEM command on the data line. The CAL_NRESET line is continually sampled at the system clock rate. When a Reset Command is determined either by

the dedicated reset line or TEM Command, the GCRC holds itself in Chip Reset for 15 clock cycles Figure 7 shows that the Reset is determined by sampling a high CAL_NRESET line followed by three successive low CAL_NRESET samples.

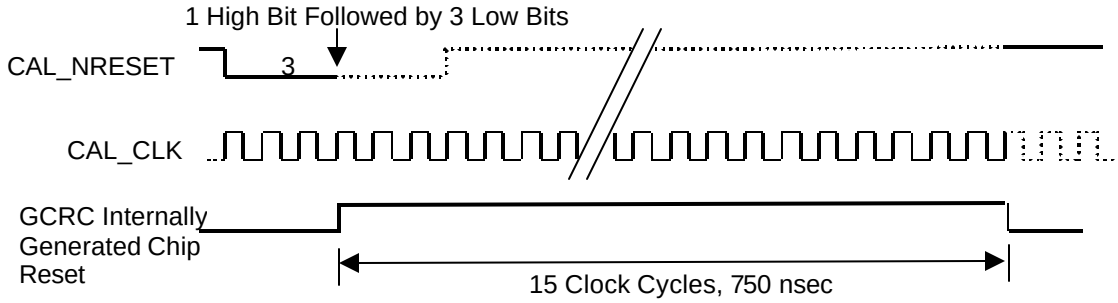


Figure 7: GCRC Reset Line Operation

Table 3 shows the effect of reset upon the GCRC registers. Registers constructed from Single Event Upset immune flip-flops are not clearable, and thus do not get changed by Reset.

Table 3: GCRC Register Reset Operation

Register	Reset Function
Time Delay 1, Peak Hold to GCFE Range decision	Register unchanged
Time Delay 2, GCFE Range decision to ADC sample	Register unchanged
Time Delay 3, ADC Conversion time	Register unchanged
Digital to Analog Converter (DAC) setting	Zero register
GCRC configuration register	Zero 3 least significant bits. GCRC version bits fixed.
Status Register	Zero register
Last Command Error Register	Zero register.

8.5 Thermistor Connections

The AFEE has connections for two thermistors for temperature monitoring whether the AFEE is powered or not. The AFEE passes the thermistor signals directly to the TEM and the TEM must be powered to monitor these temperatures. The thermistor interface is depicted in Figure 8. Thermistor placement on the AFEE X-boards and Y-boards are shown in Figure 9 and Figure 10, respectively (all dimensions are approximate).

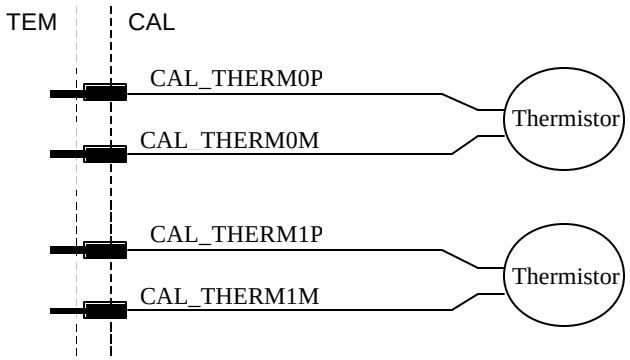


Figure 8: AFEE Thermistor Signal Interface

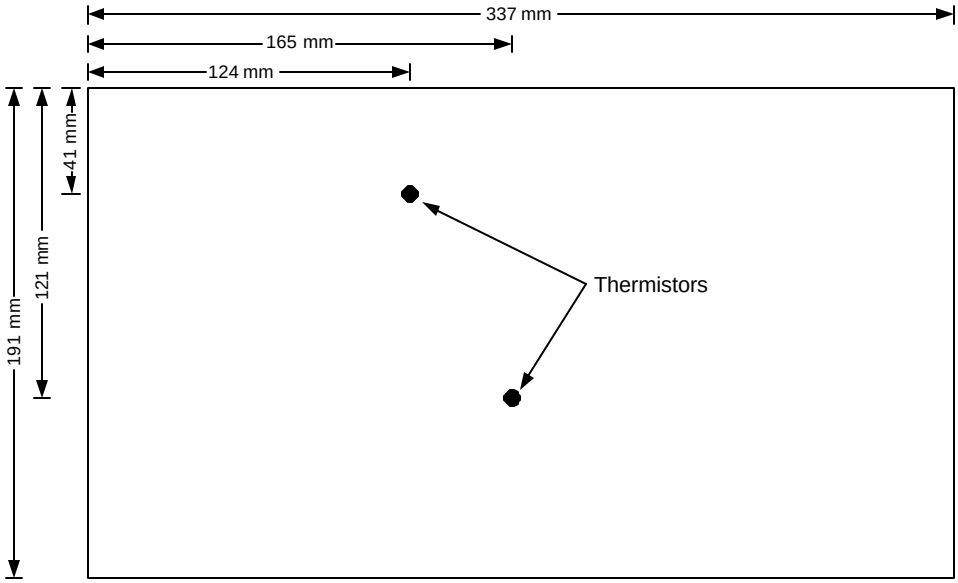


Figure 9: AFEE X-Board Thermistor Placement

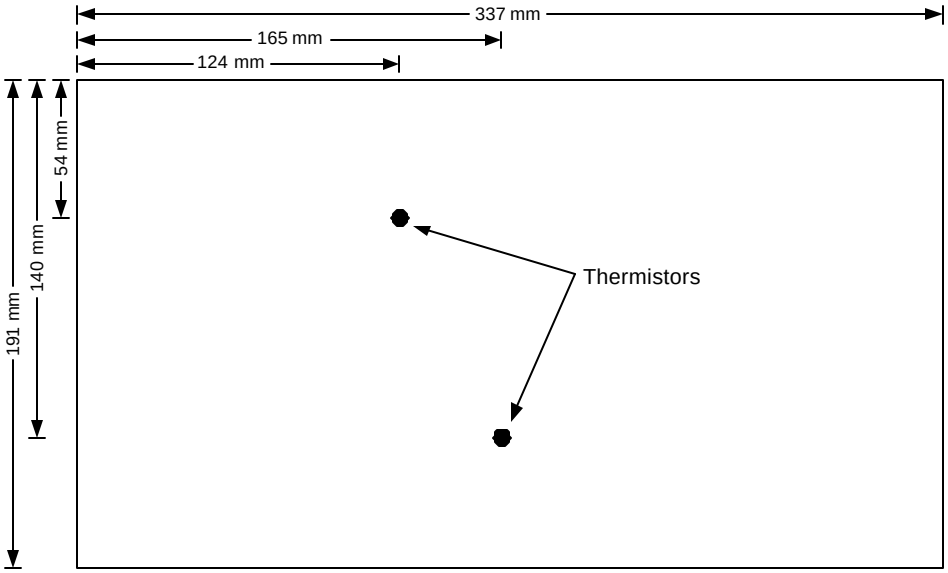


Figure 10: AFEE Y-Board Thermistor Placement

8.6 Power Consumption

Maximum power draw for the combined digital and analog 3.3V interfaces is 1.25 watts per AFEE card.

Maximum power draw for the PIN photodiode bias supply is 0.001 Watts.

8.7 Grounding and Shielding

Calorimeter Module grounding and shielding requirements shall be as defined in LAT-MD-00272, CAL Module Grounding and Shielding Plan and LAT-SS-00291, LAT Grounding and Shielding Plan.

8.8 EMI/EMC

The EMI/EMC performance is specified in the LAT-SS-00778, LAT Environmental Specification.

9 COMMANDING

Each CAL Module contains a total of four AFEE boards. There is a separate command interface from the TEM to each AFEE board. The command interface consists of two control signals: a free-running 20 MHz system clock, CAL_CLK, and a single command line, CAL_NCMD. Telemetry from each AFEE board consists of eight parallel data lines with root name CAL_NDATA. The eight data lines are clocked synchronously to the 20 MHz system clock and are partitioned as two lines per AFEE row. A reset line to the CAL Module, CAL_NRESET, forces the electronics to a known zero state. All of the commanding signals are differential LVDS format, with the CAL_NCMD, CAL_NRESET, and CAL_NDATA lines asserted low.

9.1 Command Format

The CAL Module command format consists of three bits, plus parity, followed by address on the CAL_NCMD line, sampled on the rising edge of CAL_NCLK:

- Start bit – A low level on CAL_NCMD signals the beginning of a command
- Trigger/Control bit –
  - A high level signals Command Register Load/Read
  - A low level signals a Command Signal Readout (Trigger)
- Trigger Type bit – Used only for the Command Signal Readout
  - A high level signals 1 Range Readout
  - A low level signals 4 Range Readout
- Odd Parity bit

Figure 11 shows details of the CAL Module Command format.

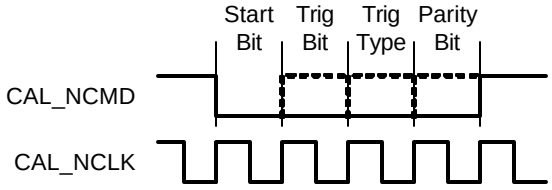


Figure 11: CAL Module Command Format

9.2 Command Types

All CAL Module commands can be categorized into three different types:

1. Command Register Load – Used for configuring the GCRC and GCFE device registers. Through address bits in the TEM command, the Load command can address:
   a. a particular GCRC or GCFE;
   b. an entire row of GCFEs;
   c. an entire column of GCFEs;
   d. or, the entire AFEE board.
2. Command Register Read – Read commands are used for verifying GCRC and GCFE registers, and for receiving returned status information.
3. Command Signal Readout (Trigger) – Used for reading out the crystal end analog data.

9.2.1 Command Register Access

Command Register accesses are defined by a high level on the CAL_NCMD line immediately following the Start bit, as shown in Figure 12. The third bit is "don't care" for register accesses, and the next bit is command parity. Following the parity bit is the actual register address, function definition, and data field (if required). The type of Command Register access, (read or write), is defined by the Function code itself. The format of the bitstream is detailed as follows:

- Address field – 9 bits
  - 4 bits GCRC address (0-3)
  - 1 bit GCFE Command Identifier, asserted = GCFE Command
  - 4 bit GCFE Address (0-11)
- Function code – 5 bits (Refer to Section 9.3)
- Address/Function parity bit
- Data Field – 16 bits
- Data parity bit

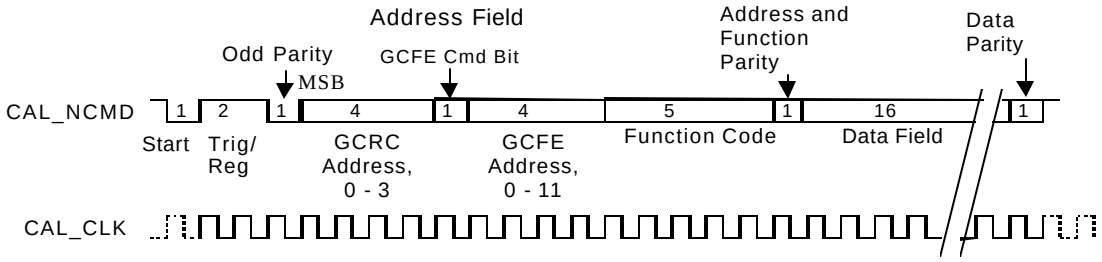


Figure 12: AFEE Command Register Access

9.3 Function Code Description

Table 4 defines the Function Code definitions for the AFEE cards. The first two columns show the address space reserved for the GCRC function bit mapping:

- For GCRC ver 4 and earlier, the first bit of the 5 bit function field indicates read - bit "1", or write - bit "0"
- For GCRC ver 5 and later, the first two bits of the 5 bit function field indicates read – bits "10", write "01", or dataless command "00"

The number of effective data bits, (number of register bits) is shown in the column to the right. For writes and reads of less than 16 data bits, the data word most significant bits are packed with zeroes. Pass-through commands from the GCRC to the GCFE are shown in *italics*.

Table 4: CAL Module Command Definitions

GCRC Ver <=4 Function Bits	GCRC Ver >=5 Function Bits	Definition	Data Bits 15-8 Write Key	Number of Data Bits
00000	00000	Write not used		
Not used	00001	Write Reset GCRC		0
00011	00011	Calibration strobe command		0
01000	*01000*	*Write GCFE Config Reg 0*		*13 bits*
10000	*10000*	*Read GCFE Config Reg 0*		
01001	*01001*	*Write GCFE Config Reg 1*		*7 bits*
10001	*10001*	*Read GCFE Config Reg 1*		
01010	*01010*	*Write GCFE Fast Low Energy DAC*		*7 bits*
10010	*10010*	*Read GCFE Fast Low Energy DAC*		
01011	*01011*	*Write GCFE Fast High Energy DAC*		*7 bits*

GCRC Ver <=4 Function Bits	GCRC Ver >=5 Function Bits	Definition	Data Bits 15-8 Write Key	Number of Data Bits
10011	*10011*	*Read GCFE Fast High Energy DAC*		
01100	*01100*	*Write GCFE Log Accept DAC*		*7 bits*
10100	*10100*	*Read GCFE Log Accept DAC*		
01101	*01101*	*Write GCFE Upper Level Discrim DAC*		*7 bits*
10101	*10101*	*Read GCFE Upper Level Discrim DAC*		
01110	*01110*	*Write GCFE Reference DAC*		*7 bits*
10110	*10110*	*Read GCFE Reference DAC*		
01011	01011	Write Time Delay 1, Peak Hold to GCFE Range decision		6 bits
11011	10011	Read Time Delay 1, Peak Hold to GCFE Range decision		6 bits
01100	01100	Write Time Delay 2, GCFE Range decision to ADC sample		6 bits
11100	10100	Read Time Delay 2, GCFE Range decision to ADC sample		6 bits
01101	01101	Write Time Delay 3, ADC Conversion time		8 bits
11101	10101	Read Time Delay 3, ADC Conversion time		8 bits
01110	01110	Write Digital to Analog Converter (DAC) setting		16 bits
11110	10110	Read Digital to Analog Converter (DAC) setting		16 bits
01111	01111	Write GCRC configuration register	A5	3 bits
11111	10111	Read GCRC configuration register. GCRC Version Number is 8 most significant bits.		3 bits
10000	10000	Read Status Register		5 bits
10001	10001	Read Last Command Error		16 bits

9.4 Command Register Load

The AFEE hardware has a limit on how closely spaced in time it can handle successive commands. Figure 13 shows that the definition in spacing that will be used is the time between the last bit transmitted from the first command and the time in which the start bit is transmitted in the second command. The minimum successive delays are defined in Table 5. It is expected that for GCRC versions greater than 1, the minimum time for successive GCFE writes will be reduced to the same 3 clock cycles as for the other commands.

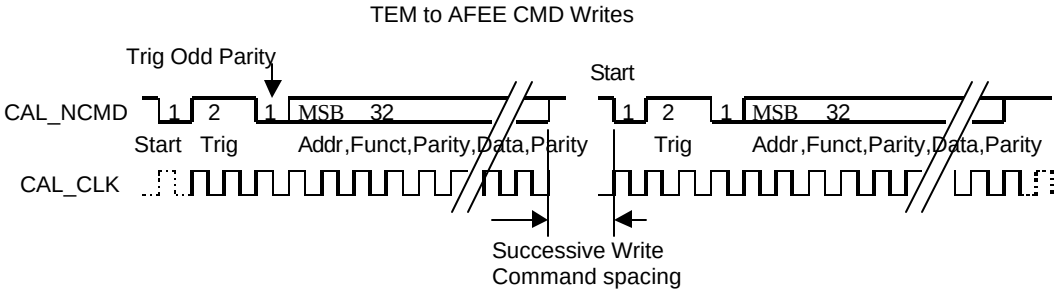


Figure 13: AFEE Command Register Load Timing

Table 5: Minimum Successive Write Delays

First Action	Second Action	Minimum Delay
GCRC Write	GCRC Read/Write, GCFE Read/Write or Readout	3 Clk Cycles
GCFE Write	GCRC Read/Write, GCFE Read/Write or Readout	15 Clk Cycles (GCRC Ver. 1)
DAC Write	GCRC Read/Write, GCFE Read/Write or Readout	3 Clk Cycles
DAC Write	DAC Write	33 Clk Cycles

9.5 Command Register Read

Figure 14 shows the command structure and response delay definition for AFEE read commands. The command structure is similar to the load commands, but shorter without a required data field or data parity. The command reply repeats the address and function bits, adds parity according to the particular GCRC configuration register, follows with 16 bits of data, status error flag, and then data-status error parity. The maximum and minimum read response delay values are shown in Table 6.

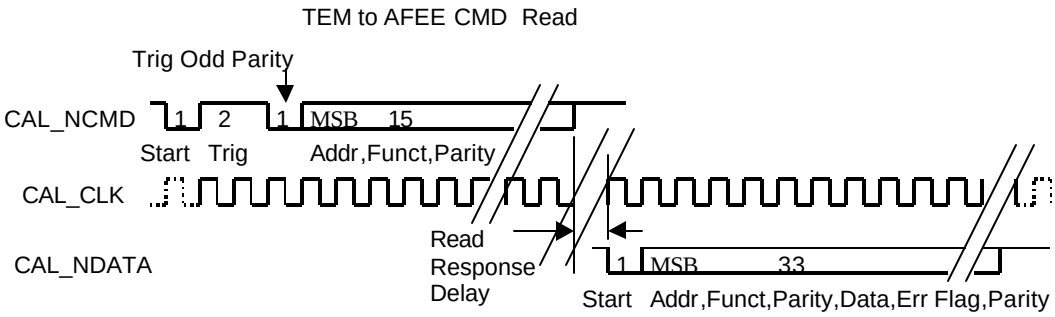


Figure 14: AFEE Command Register Read Timing

Table 6: Read Response Delay Values

Action	Min Delay	Max Delay
GCRC Read	3 Clk Cycles	3 Clk Cycles
GCFE Read	15 Clk Cycles	40 Clk Cycles (GCFE Response Timeout)
DAC Read	3 Clk Cycles	3 Clk Cycles

9.6 GCRC Register Access

9.6.1 Last Command Error Register

The GCRC Last Command Error Register bit definitions are listed in Table 7. The MSB (Bit 15) defines whether the remaining stored command bits begin with the TEM Trigger bits, or with the TEM Address bits.

Table 7: GCRC Last Command Error Register Bit Definition

Bit 15 (MSB)	Bit 14 – Bit 0
0	2 Trig Bits, 1 Trig Parity Bit, 9 Address Bits, 3 Function Bits
1	9 Address Bits, 5 Function Bits, 1 Address-Function Parity Bit

9.6.2 GCRC Configuration Register

The GCRC Configuration Register bit definitions are listed in Table 8. Three bits are used to define the parity in the configuration register to reduce probability of communication failure due to single event upset.

Table 8: GCRC Configuration Register Bit Definition

Bit	Definition
0 (LSB)	GCRC Parity Bit A, default value 0
1	GCRC Parity Bit B, default value 0
2	GCRC Parity Bit C, default value 0

Note: Default Parity is Odd, at least one of Parity Bit A, B, C is value 0.
Even Parity is all Parity Bits A, B, and C set to 1.

9.6.3 GCRC Status Register

The GCRC Status Register bit definitions are listed in Table 9.

Table 9: GCRC Status Register Bit Definition

Bit	Definition
0 (LSB)	TEM Trigger Parity Error occurred
1	TEM Commmand Address and Function Parity Error occurred
2	TEM Data Parity error occurred
3	GCFE Read Timeout
4	TEM Command Error. Commanded address and parity correct, but not recognized, write, or dataless function command.

9.7 Calibration DAC Access

Each CAL Module AFEE board has one 12 bit calibration Digital to Analog Converter (DAC) per row. The 12 bit DAC is the Maxim MAX5121, which has an output voltage range between zero and 1.25 volts and is wired to power up at the midrange voltage of 0.61 volts.

The DAC is programmed by a 5 MHz serial data stream from the GCRC. As the GCRC is pushing data bits into the onboard DAC, the previous DAC-held data bits, DAC_DATA_IN, are received by the GCRC. A subsequent TEM DAC Read command returns these previous DAC data bits, the bits pushed out by the last DAC Write command. Thus a TEM DAC Read command returns the second-to-last DAC Write command. Successive DAC Read commands return the same value.

Each row's DAC is programmed through 16-bit commands to that row's GCRC chip - 3 bits for control, 12 DAC data bits, and a zero bit, passed directly through the GCRC chip. The command bit definitions are shown in Table 10.

Table 10: Onboard DAC Programming Bits

B15 (MSB)	B14	B13	B12-B1	B0 (LSB)	Description
0	0	0	Don't Care	0	No Operation
0	1	0	12 Bit DAC value	0	DAC Write

The timing of the DAC read command is the same as any GCRC register – reference Section 9.5 for details. The timing of the DAC Write operation is longer due to the reduced rate serial communication, and is shown in Figure 15. The GCRC will accept any TEM command immediately following a DAC Write command except another DAC Write.

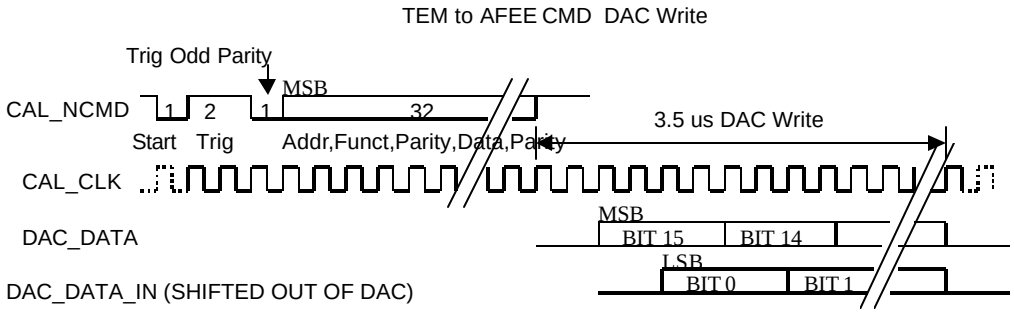


Figure 15: DAC Write Command Timing

9.8 Calibration Strobe Command

The Calibration Strobe Command is used to calibrate the Calorimeter front-end electronics by commanding the GCRC to assert the CALIB_STRB signal to inject an amount of charge proportional to the external DAC voltage setting, into the row of GCFE preamplifiers. Figure 16 shows that the GCRC asserts the CALIB_STRB signal to the row of GCFE chips immediately following reception of the Calibration command from the TEM. The CALIB_STRB is a fixed pulse

width of 6.2 microseconds, long enough that the analog signal is sampled prior to the falling edge of CALIB_STRB. The TEM may command a trigger request to the GCRC during the CALIB_STRB asserted high period, therefore the GCRC will be able to process further commands or trigger requests from the TEM during the Calibration pulse period.

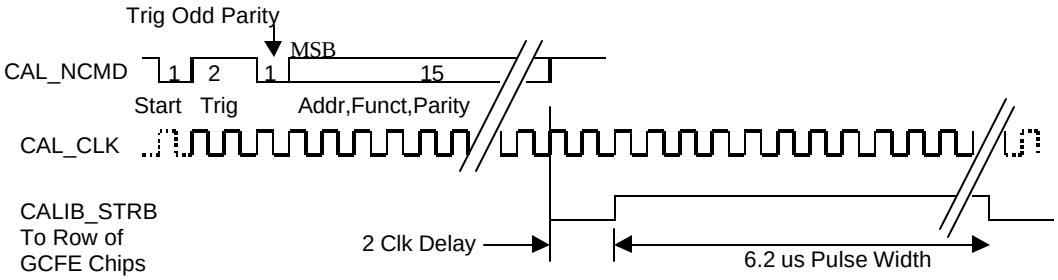


Figure 16: TEM Calibration Command

9.9 Signal Readout

The nominal readout operation is digitization of one of the four possible GCFE ranges per log end. The Trigger command from the TEM can specify readout of one or all four GCFE ranges (Reference Table 9-1). For single range readout, the GCFE chips are nominally allowed to decide their individual optimum range to readout per event, based upon crystal-end signal level. Thus for correct association of the ADC data, AFEE sends two range definition data bits per range digitized. The range definition bits are passed with the ADC data to the TEM.

Zero suppression, the process of discarding minimal amplitude data, is made easier with a dedicated discriminator bit in each GCFE chip. The log-accept bit is again passed with the ADC data, enabling the TEM to quickly zero suppress data with no computation.

Figure 17 shows signal command for range readout operation. Table 11 defines the bits for requesting 1 or 4 range readout.

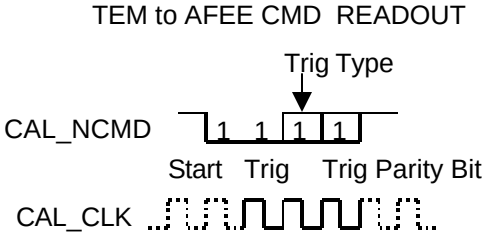


Figure 17: Command Signal Readout Timing

Table 11: Readout (Trigger) Type Bit Definitions

Bit Value	Definition
0 high	1 Range Readout
1 Asserted Low	4 Range Readout

The data returned by the AFEE from the readout command follows a preset order so that the TEM can associate data with log-ends. The AFEE always transmits all the log-end information. Figure 18 shows the general log-end readout order per AFEE row, for sides with the RIGHT_FIRST not asserted, +X and +Y sides. Figure 19 shows the general log-end readout order per AFEE row for the RIGHT_FIRST asserted sides, -X and –Y sides. Figure 20 shows the interleaving of the readout data bits per AFEE row, in transmission to the TEM, for the non RIGHT_FIRST asserted sides. Figure 21 shows the interleaving of the readout data bits per AFEE row, in transmission to the TEM, for the RIGHT_FIRST asserted sides Figure 22 shows the data packet organization for 4 range readout, which has four separate data packets transmitted to the TEM, of two different bit lengths.

Figure 18: Generalized Log-End/ADC Data Return Order, per row (Right_First not asserted)

Figure 19: Generalized Log-End/ADC Data Return Order, per row (Right_First asserted)

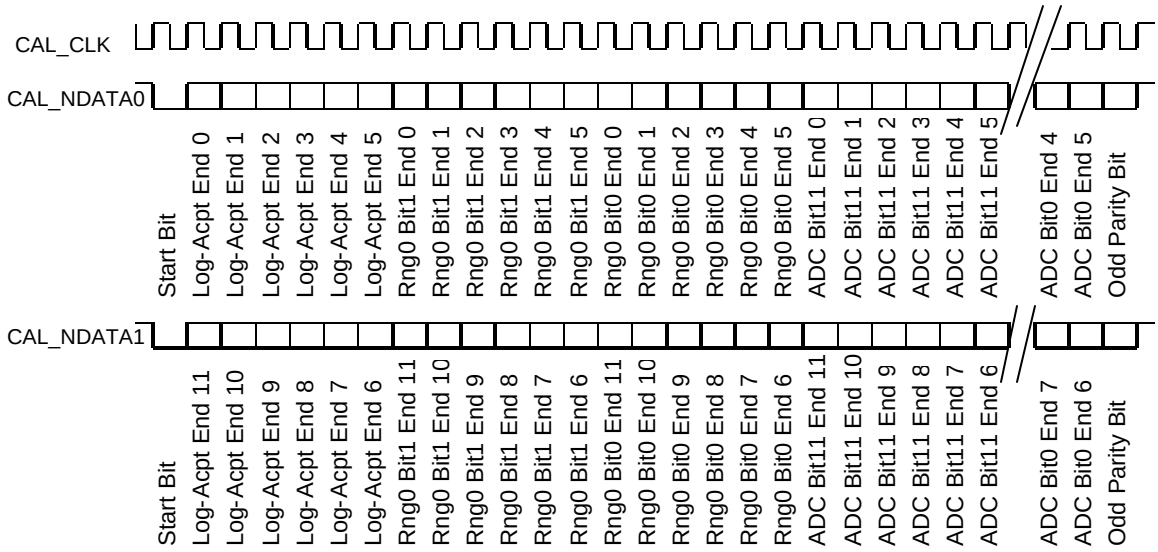


Figure 20: Interleaved Log-End/ADC Data Formatting per row, Single Range Readout, Right_First Not Asserted

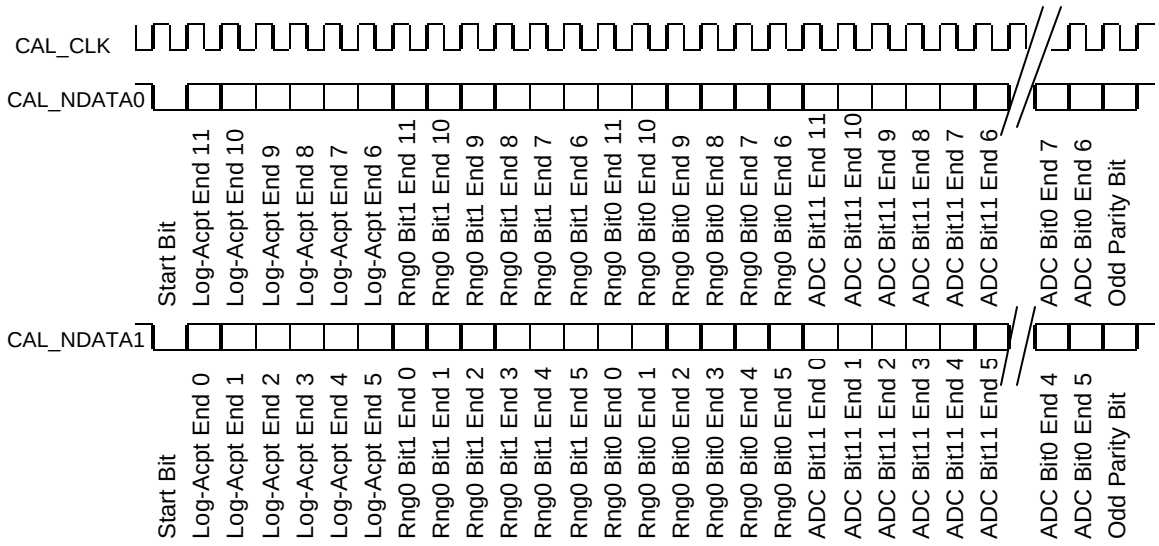


Figure 21: Interleaved Log-End/ADC Data Formatting per row, Single Range Readout, Right_First Asserted

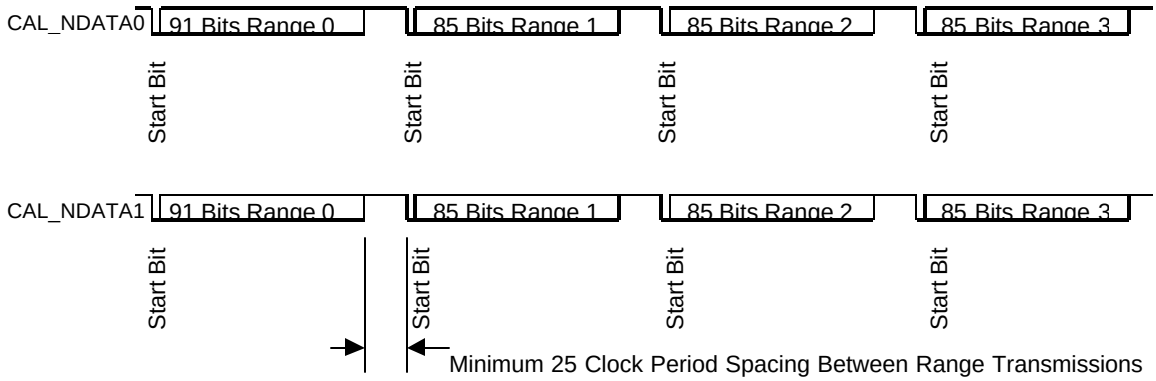


Figure 22: Log-End/ADC Data Formatting per row, Four Range Readout

(Note that ranges 2 to 4 do not send log-accept bits)

10 THERMAL INTERFACE and HEAT TRANSFER

10.1 CAL Requirements

The bolted joint interface with the Grid shall be the primary mechanism for transferring heat into and out of the CAL. This interface should have an overall conductance > 0.03 watts/sq cm deg C.

The CAL shall meet the temperature requirements in the LAT Environmental Specification, LAT-SS-00778, Section 11.3, Temperature Limits.

Instrumentation (thermocouples, thermisters, etc) used for test are defined in LAT-TD-00890, LAT Instrumentation Plan.

10.2 LAT Requirements

The LAT Grid and the LAT thermal control system shall maintain the Cal modules within the temperatures shown in the LAT Environmental Specification, LAT-SS-00778, Section 11.3, Temperature Limits..

10.3 CAL to TEM Thermal Interface and Heat Transfer

The interface conductance between the CAL and TEM/PS box is 0.1 W/deg C total. The CAL to TEM radiative interchange will be based upon low emissivity (<0.1) surface finishes for both the CAL and TEM. The CAL surface finish shall be alodine (MIL-C-5541, Class 3) except for the CAL tabs and the surrounding region as shown in the CAL-LAT IDD, LAT-DS-00233. The bounding TEM temperatures will be based upon acceptance test temperatures from the LAT Environmental Specification, LAT-MD-00778.

10.4 CAL to TKR Thermal Interface and Heat Transfer

The top of the CAL module and underside of the bottom tray of the TKR module are radiatively coupled. The bottom tray of the Tracker module shall have a low emissivity (<0.1) surface finish. The CAL surface finish shall be a low emissivity (<0.1) alodine finish (MIL-C-5541, Class 3) except for the CAL tabs and the surrounding region as shown in the CAL-LAT IDD, LAT-DS-00233. The LAT grid will have a high emissivity coating (0.75 < emissivity < 0.9). The maximum temperature difference between the CAL and Tracker bottom tray will be 10°C.

11 CABLE ROUTING and SUPPORT

The following subsections contain information pertaining to cable routing and support and their effects to the CAL-LAT interface. Additional detail is available in the CAL Outline Drawing, LAT-DS-001625.

11.1 CAL Module – TEM Cables

Each CAL Module-TEM cable passes between the tabs at the CAL base plate-Grid interface. A CAL-TEM cable bracket (machined aluminum) provides support and strain relief for each cable. Four CAL-TEM cable brackets are mounted, one on each side, to the –Z surface of each CAL base plate.

11.2 Tracker Kapton Flex-Circuit Cables

Each Tracker tower has eight kapton flex-circuit cables that pass between the tabs at the CAL base plate-Grid interface. The exact locations are shown in the CAL-LAT IDD, LAT-DS-00233. No Tracker cable support or strain relief points are located on the CAL base plate.

11.3 Electronic Box Cable Trays

A network of cable trays are used to provide support and strain relief of the cabling for the SIU's, GASU, PDU, EPU's, and TEM's. The cable tray network consists of bridges (machined 6061-T6 aluminum), T transition plates (5052 aluminum), X transition plates (5052 aluminum), and the cable trays (5052 aluminum). Only the bridges interface with the Cal base plate . The bridges mount to the CAL base plate using the existing GSE holes located in each corner. The mounting hardware consists of M8 x 18mm Socket Head Cap Screws. Figure 23 shows a portion of the cable tray network.

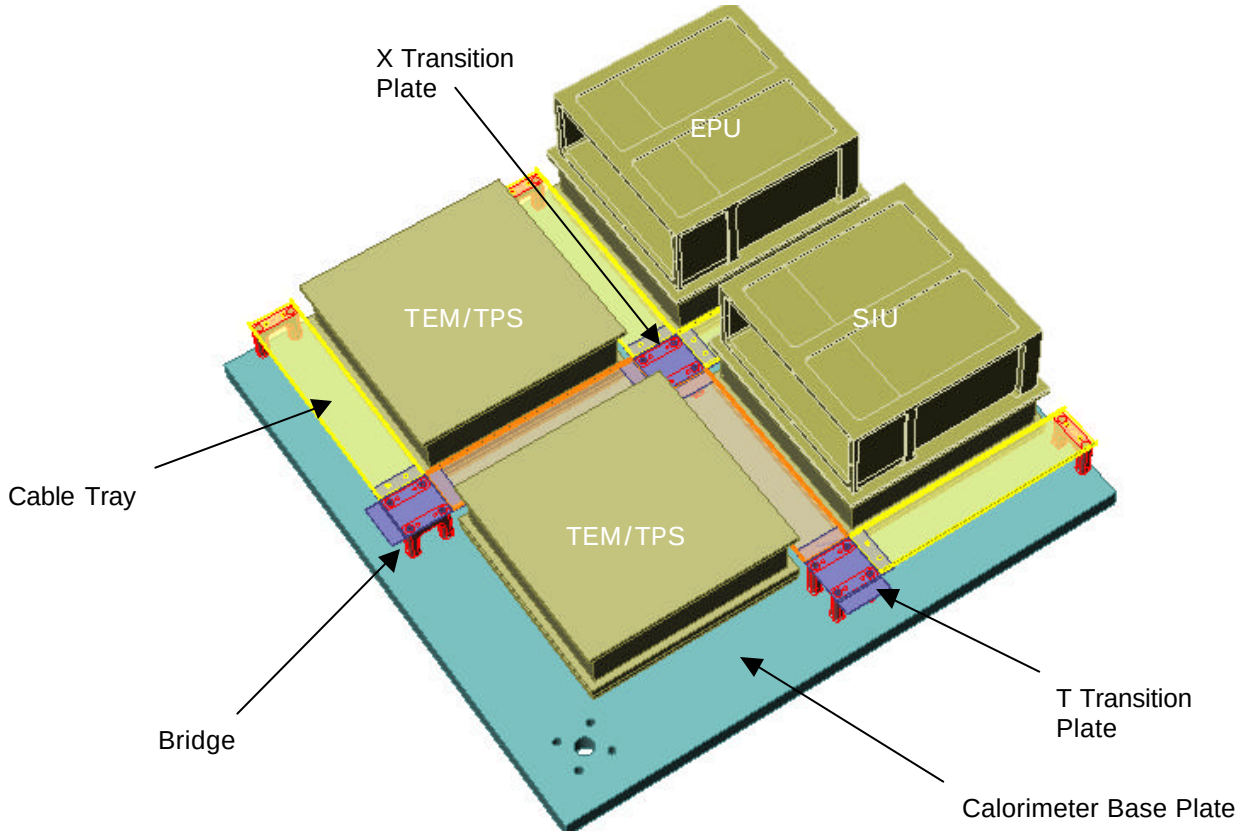


Figure 23: Cable Tray Concept

12 INTEGRATION and TEST INTERFACES

12.1 Integration Stay-Clears and Access Requirements

The CAL module is nominally mounted in the Grid with a Power Supply and TEM attached.
Any CAL module shall be capable of being integrated into any Grid bay in the LAT.

Any CAL module shall be capable of being de-integrated from the Grid at any time with no need to remove or invalidate verification of neighboring modules.

GSE attachment points can be accessed during instrument I&T without invalidation of installed modules.

The Grid shall provide a minimum of 0.7 mm gap on all four sides of the CAL module during integration. This space will be used only for integration and alignment allowance. Thus, when the CAL is integrated, the 0.7 mm gap will be used to correct for tolerances of position location in the mating features.

During CAL integration, there is NO access available from the front face ("top") of the Grid due to the tracker.

The CAL shall be capable of being integrated vertically, either from underneath the Grid, or being lowered down from above an inverted Grid.

12.2 Provision for Alignment and Surveying

During CAL integration, there are NO surveying lines-of-sight available from the front face of the Grid.

CAL modules are not capable of being aligned after integration on the Grid.

No survey of the CAL modules is required during instrument I&T.

12.3 Integration GSE

LAT I&T will provide all GSE related to alignment and installation of calorimeter modules during instrument I&T. GSE will guarantee no contact with CAL module prior to base plate contact with Grid in final attachment configuration.

12.3.1 Calorimeter Responsibilities

12.3.1.1 MGSE

The following NRL-supplied Mechanical Ground Support Equipment (MGSE) is required for environmental testing and integration of the CAL to the LAT:

- Handling Fixture – Handling Fixture Plate with exterior dimensions and the required interface for the SLAC provided lift fixture as defined in NRL Drawing B8677, Rev. A, Base Plate, Handling Fixture, GLAST. Four GSE Support Rods, located as specified in the CAL-LAT IDD, LAT-DS-00233
- Lift Fixture/Spreader Bar – required to hoist the CAL module, with its + Z axis pointing opposite the gravity vector, onto the SLAC provided Calorimeter Rotation Fixture prior to integration
- Shipping Container – used to secure and provide humidity control for the CAL Module during shipment

13.3.1.2 EGSE

The only NRL-supplied EGSE required for environmental testing of the CAL Module are:

- Special test cables used to interface the CAL Module to LAT-provided EGSE during Environmental testing

12.3.2 LAT Responsibilities

12.3.2.1 MGSE

The following SLAC-supplied MGSE is required for integration of the CAL to the LAT:

- Calorimeter Rotation Fixture - required to rotate the CAL module so that its +Z axis is pointing downward for integration.
- Calorimeter Lift Fixture - required for lowering the CAL module into the LAT Grid.
- Calorimeter Alignment Tool - to ensure no contact between the Calorimeter's exterior housing and the interior surface of each respective LAT Grid Bay during integration.

12.3.2.2 EGSE

The following SLAC-supplied EGSE is required to support testing of the CAL Module during Qualification and Acceptance level testing, and Post-Ship Acceptance testing:

- TEM Electronics CAL Module electrical test set – used to monitor operation of CAL Module during Environmental testing
- TEM Electronics Connector Savers – used to protect flight connectors when connecting test cabling to the TEM Flight unit during Environmental testing. The current baseline is to provide TEM EM2 to support CAL Module testing. In which case, no TEM connector savers will be provided.

13 OTHER INTERFACES

13.1 Venting

During launch, air from a CAL module shall be vented down, past the bottom plate, and not up into the volume between the TKR and CAL.

13.2 Particulates

The CAL shall contain all fracture-sensitive materials such that any particulates produced by a fracture shall be contained within the stay-clear volume of the CAL.

13.3 Humidity

The cesium iodide crystals of the CAL are sensitive to moisture. As per LAT-MD-00404, LAT Contamination Control Plan, the relative humidity in the air surrounding the calorimeter will not exceed 45%. The LAT Contamination Control Plan contains provisions for a dry air or nitrogen purge to meet the relative humidity requirement. Due to ESD concerns, all work near the LAT, including the calorimeter, will cease if the relative humidity is less than 30%.